NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND ITS MANUFACTURING METHOD

CROSS REFERENCE TO RELATED APPLICATION

This application claims benefit of priority under 35USC §119 to Japanese Patent Application No. Hei 11-350841(1999), filed on December 9, 1999, the entire contents of which are incorporated by reference herein.

BACKGROUND OF THE INVENTION

This invention relates to a nonvolatile semiconductor memory device and its manufacturing method.

There is known an electrically rewritable, nonvolatile semiconductor memory (EEPROM: electrically erasable and programmable read-only-memory) using memory cells of a stacked-gate structure stacking floating gates and control gates. This kind of EEPROM uses a tunneling insulation film as a first gate insulating film between floating gates and a semiconductor substrate and typically uses, as the second gate insulating film between floating gates and control gates, an ONO film which is a multi-layered film of a silicon oxide film (O) on a silicon nitride film (N) on a silicon oxide film (O).

Each memory cell is formed in an element-forming region partitioned by an element isolation/insulation film. In general, a floating gate electrode film is divided in the direction of control gate line (word line) by making a slit on the element isolation/insulation film. In the step of making the slit, division of floating gates in the bit-line direction is not yet done. Then a control gate electrode film is stacked via an ONO film on all surfaces of the substrate including the top of the slit-processed floating gate electrode film, and by sequentially etching the control gate electrode film, ONO film, and floating gate electrode film, control gates and floating gates are isolated in the bit-line direction. After that, source and drain diffusion layers are formed in self-alignment with the control gates.

In the above-introduced conventional EEPROM structure,

floating gates of memory cells adjacent in the word-line direction are isolated on the element isolation/insulation film, but the ONO film formed thereon is continuously made in the word-line direction. It is already known that, if the isolation width (slit width) of floating gates in the word-line direction is narrowed by miniaturization of memory cells, this structure is subject to movements of electric charges through the ONO film when there is a difference in charge storage status between adjacent floating gates. This is because electric charges are readily movable in the lateral direction in the silicon nitride film or along the boundaries between the silicon nitride film and the silicon oxide films of the ONO film. Therefore, in microminiaturized EEPROM, when adjacent memory cells in the word-line direction have different data states, their threshold values vary due to movements of electric charges, and often result in destruction of data.

SUMMARY OF THE INVENTION

It is therefore an object of the invention to provide a nonvolatile semiconductor memory device improved in reliability by preventing destruction of data caused by movements of electric charges between floating gates, and also relates to its manufacturing method.

According to the first aspect of the invention, there is provided a nonvolatile semiconductor memory device comprising:

a semiconductor substrate;

a plurality of element-forming regions partitioned by element isolation/insulation films in said semiconductor substrate;

floating gates formed in said element-forming regions via a first gate insulating film and separated for individual said element-forming regions;

second gate insulating films formed on said floating gates, and divided and separated above said element isolation/insulation films;

control gates formed on said floating gates via said second gate insulating films; and

source and drain diffusion layers formed in self-alignment with said control gates.

According to the second aspect of the present invention, there is provided a nonvolatile semiconductor memory device comprising:

a semiconductor substrate;

a plurality of element-forming regions partitioned by element isolation/insulation films in said semiconductor substrate;

floating gates formed in said element-forming regions via a first gate insulating film and separated for individual said element-forming regions;

a second gate insulating film formed on said floating gates to continuously extend over a plurality of element-forming regions along recesses made into surfaces of said element isolation/insulation films;

control gates formed on said floating gates via said second gate insulating film; and

source and drain diffusion layers formed in self-alignment with said control gates.

According to the third aspect of the present invention, there is provided a manufacturing method of a nonvolatile semiconductor memory device, comprising the steps of:

making element isolation/insulation films that partition element-forming regions in a semiconductor substrate;

stacking a first gate electrode material film and a second gate insulating film on said semiconductor substrate via a first gate insulating film;

etching said second gate insulating film and the underlying first gate electrode material film to make slits that separate said first gate electrode material film above said element isolation/insulation films;

forming an insulating film on side surfaces of said first gate electrode material film, and thereafter stacking a second gate electrode material film;

sequentially etching said second gate electrode material film, said second gate insulating film and said first gate

electrode material film to pattern said first gate electrode film into floating gates and said second gate electrode material film into control gates; and

making source and drain diffusion layers in self alignment with said control gates.

According to the fourth aspect of the present invention, there is provided a manufacturing method of a nonvolatile semiconductor memory device, comprising the steps of:

making element isolation/insulation films that partition element-forming regions in a semiconductor substrate;

stacking a first gate electrode material film and a second gate insulating film on said semiconductor substrate via a first gate insulating film;

etching said second gate insulating film and the underlying first gate electrode material film to make slits that separate said first gate electrode material film above said element isolation/insulation films;

sequentially stacking a third gate insulating film and a second gate electrode material film;

sequentially etching said second gate electrode material film, said third and second gate insulating films, and said first gate electrode material film to pattern said first gate electrode material film into floating gates and said second gate electrode material film into control gates; and

making source and drain diffusion layers in self-alignment with said control gates.

According to the fourth aspect of the present invention, there is provided a manufacturing method of a nonvolatile semiconductor memory device, comprising the steps of:

making element isolation/insulation films that partition element-forming regions in a semiconductor substrate;

stacking a first gate electrode material film on said semiconductor substrate via a first gate insulating film;

etching said first gate electrode material film to make slits that separate said first gate electrode material film on said element isolation/insulation films;

etching surfaces of said element isolation/insulation

films exposed to said slits to make recesses;

stacking a second gate electrode material film on said first gate electrode material film and said element isolation/insulation films via said first gate insulating film;

sequentially etching said second gate electrode material film, said gate insulating film and said first gate electrode material film to pattern said first gate electrode material film into floating gates and said second gate electrode material film into control gates; and

making source and drain diffusion layers in self-alignment with said control gates

According to the invention, by isolating the second gate insulating film between the floating gates and the control gates in a region between adjacent memory cells via an element isolation/insulation film, electric charges are prevented from moving between adjacent floating gates via the second gate insulating film.

Furthermore, even when the second gate insulating film is not completely isolated on the device isolation film, if a recess is made on the surface of the element isolation/insulation film to have the second gate insulting film extend along the recess, it is substantially equivalent to an increase of the distance between adjacent floating gates, and here again results in preventing movements of electric charges between adjacent floating gates.

Therefore, also when memory cells are miniaturized, the invention prevents data destruction due to movements of electric charges and improves the reliability.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a layout of a memory cell array of EEPROM according to Embodiment 1 of the invention;

Figs. 2A and 2B are cross-sectional views taken along the A-A' line and B-B' line of Fig. 1;

Figs. 3A and 3B are cross-sectional views for showing a manufacturing process of Embodiment 1;

Figs. 4A and 4B are cross-sectional views for showing the

manufacturing process of Embodiment 1;

Figs. 5A and 5B are cross-sectional views for showing the manufacturing process of Embodiment 1;

Figs. 6A and 6B are cross-sectional views for showing the manufacturing process of Embodiment 1;

Figs. 7A and 7B are cross-sectional views for showing the manufacturing process of Embodiment 1;

Figs. 8A and 8B are cross-sectional views for showing the manufacturing process of Embodiment 1;

Figs. 9A and 9B are cross-sectional views for showing a manufacturing process of Embodiment 2 of the invention;

Figs. 10A and 10B are cross-sectional views for showing the manufacturing process of Embodiment 2;

Figs. 11A and 11B are cross-sectional views for showing the manufacturing process of Embodiment 2;

Figs. 12A and 12B are cross-sectional views for showing the manufacturing process of Embodiment 2;

Figs. 13A and 13B are cross-sectional views for showing a manufacturing process of Embodiment 3 of the invention;

Figs. 14A and 14B are cross-sectional views for showing the manufacturing process of Embodiment 3;

Figs. 15A and 15B are cross-sectional views for showing the manufacturing process of Embodiment 3;

Figs. 16A and 16B are cross-sectional views for showing the manufacturing process of Embodiment 3;

Figs. 17A and 17B are cross-sectional views of EEPROM according to the fourth embodiment of the invention, which correspond to Figs. 2A and 2B;

Figs. 18 is a cross-sectional view for showing the manufacturing process of Embodiment 4;

Fig. 19 is a cross-sectional view for showing the manufacturing process of Embodiment 4;

Fig. 20 is a cross-sectional view for showing the manufacturing process of Embodiment 4;

Fig. 21 is a cross-sectional view for showing the manufacturing process of Embodiment 4;

Fig. 22 is a cross-sectional view for showing the

manufacturing process of Embodiment 4;

Fig. 23 is a cross-sectional view for showing the manufacturing process of Embodiment 4;

Fig. 24 is a cross-sectional view for showing the manufacturing process of Embodiment 4;

Fig. 25 is a cross-sectional view for showing the manufacturing process of Embodiment 4; and

Fig. 26 is a diagram that shows correlation between defective numbers of bits and slit widths for explaining effects of Embodiment 4.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Explained below are embodiments of the invention with reference to the drawings.

[Embodiment 1]

Fig. 1 is a layout of a cell array of NAND type EEPROM according to Embodiment 1 of the invention. Figs. 1A and 2B are cross-sectional views taken along the A-A' line and B-B' line of Fig. 1.

The memory cell array is formed on a p-type well of a silicon substrate 1. The silicon substrate 1 has formed device isolation channels 3 buried with device isolation films 4 to define stripe-shaped element-forming regions 2.

In the element-forming regions 2, floating gates 6 are formed via first gate insulating films 5 as tunneling insulation films. Floating gates 6 have a two-layered structure stacking first polycrystalline silicon (or amorphous silicon) films 6a made before isolation of devices and second polycrystalline silicon (or amorphous silicon) films 6b made after isolation of devices, and they are divided for individual memory cells. Formed on the floating gates 6 are control gates 8 via second gate insulating films 7. Control gates 8 have a two-layered structure of polycrystalline silicon (or amorphous silicon) films 8a and tungsten silicide (WSi) films 8b. The control gates 8 are patterned to continuously extend over a plurality of element-forming regions 2 in the cross-section of Fig. 2A, and they form word lines WL.

The second gate insulating films 7 between the floating gates 6 and the control gates 8 are ONO films. In this embodiment, second gate insulating films 7 are divided by slits 13 on element isolation/insulation films 4 to lie merely on floating gates 6 along word line directions in the cross-section of Fig. 2A. Therefore, on side surfaces of floating gates 6, silicon oxide films 9 are formed to isolate floating gates 6 from control gates 8.

Source and drain diffusion layers 12 are formed in self alignment with control gates 8, and a plurality of memory cells are serially connected to form NAND type cell units.

At the drain side of one-side ends of NAND type cell units, selection gates 13 formed simultaneously with control gates 8 are located, and bit lines (BL) 11 are connected to their drain diffusion layers. The selection gates 13 portion has the same multi-layered gate structure as the gate portions of memory cells, but the first gate electrode material film in that portion is not isolated as floating gates, and two layers integrally form selection gates 13 short-circuited at predetermined positions. In the selection gates 13 portion, the first gate insulating film 5' is thicker than that of the memory cell region. Although not shown, the other end source side of the NAND cell units is made in the same manner as the drain side.

A specific manufacturing process of EEPROM according to the embodiment is explained with reference to Fig. 3A and 3B through Figs. 8A and 8B, which are cross-sectional views corresponding to Figs. 2A and 2B, under different stages of the process.

As shown in Figs. 3A and 3B, first stacked on a silicon substrate 1 is a 10 nm thick silicon oxide film as the first gate insulating film 5, a 60 nm thick first polycrystalline silicon film 6a, which is a gate electrode material film, is next stacked thereon, and a mask material 21 is further stacked for device isolation processing. In the region for the gate transistors, a gate insulating film 5' thicker than that of the region for cell transistors. The mask material 21 is a multi-layered film stacking a silicon nitride film and a silicon oxide film. The

mask material 21 is patterned and left only in element-forming regions, and by using it, the polycrystalline silicon film 6a, first gate insulating film 5, 5' are etched, and the substrate 1 is additionally etched, to form device-isolating grooves 3.

After that, it is annealed in an O_2 atmosphere at 1000°C to create a silicon oxide film 22 of about 6 nm on inner walls of the device-isolating grooves 3 as shown in Figs. 4A and 4B. Subsequently, a silicon oxide film is stacked by plasma CVD and then smoothed by CMP so as to bury it as element isolation/insulation films 4 in the device-isolating grooves 3. Then, after annealing it in a nitrogen atmosphere at 900°C, the mask material 21 is removed. Removal of the silicon nitride film relies on phosphoric-acid treatment at 150°C.

After that, as shown in Figs. 5A and 5B, the second polycrystalline silicon film 6b doped with phosphorus is stacked by low-pressure CVD, and an ONO film to be used as the second gate insulating film 7 is stacked successively. Then, using a resist pattern having apertures on element isolation/insulation films 4 as a mask, the second gate insulating film 7 and the second polycrystalline silicon film 6b are etched by RIE to make slits 13 that isolate floating gates 6 on element isolation/insulation films 4 as shown in Figs. 6A and 6B. The slits 13 have a length enough to extend through a plurality of memory cells in the NAND cell unit. Differently from prior art techniques, the second gate insulating film 7 is simultaneously isolated by slits 13 on the element isolation/insulation films 4.

Side surfaces of the polycrystalline silicon film 6b exposed by formation of slits 13 are protected by heating the structure in an O2 atmosphere at 1000°C and thereby creating a silicon oxide film 9. After that, as shown in Figs. 7A and 7B, a polycrystalline silicon film 8a dopes with phosphorus is stacked as the gate electrode material film by CVD, and a WSi film 8b is successively stacked thereon.

A resist is next applied and patterned, and the WSi film 8b, polycrystalline silicon film 8a, gate insulating film 7, polycrystalline silicon films 6b, 6b, and gate insulating film 5 are sequentially etched to make control gates 8 in the pattern

of continuous word lines WL, and divide the floating gates 6 into discrete forms in the bit-line direction. Thereafter, by ion implantation, source and drain diffusion layer 12 in self-alignment with the control gates 8 are formed for individual memory cells.

As to the selection gate line SG, the lower gate electrode material films 7a, 6b are not divided on the element isolation/insulation films 4, but they are continuously patterned integrally with the upper gate electrode material films 8a, 8b.

Thereafter, as shown in Figs. 2A and 2B, an inter-layer insulating film 10 is stacked, contact holes are made, and bit lines 11 are stacked and patterned.

As explained above, according to the embodiment, the second gate electrode material film in form of ONO film on floating gates 6 is divided simultaneously with the floating gates 6 on the element isolation/insulation films 4. Therefore, even in a structure where floating gates of adjacent memory cells are closely located, leakage of electric charges does not occur, and data is reliably kept in each memory cell.

[Embodiment 2]

Figs. 9A and 9B through Fig. 12A and 12B show a manufacturing process according to another embodiment. Parts or elements corresponding to those of the former embodiment are labeled with the common reference numerals, and their detailed explanation is omitted. Also in this embodiment, the second gate insulating film 7 in form of ONO film on the floating gates 6 is divided on the element isolation/insulation films 4, but its process is different from the former embodiment.

Up to the step shown in Figs. 5A and 5B, the process is the same as that of the former embodiment. After that, as show in Figs. 9A and 9B, a silicon oxide film 31 is stacked on the second gate insulating film 7, and slit-making apertures 13' are opened on the element isolation/insulation films 4. Further stacked thereon a silicon oxide film 32. It then undergoes etching-back to be maintained side spacers only in the apertures 13' as shown in Figs. 10A and 10B. In this status, using the

silicon oxide films 31, 32 as a mask, the second gate insulating film 7 and the polycrystalline silicon film 6b are etched by RIE. As a result, similarly to the former embodiment, slits 13 are made to divide the second gate insulating film 7 and the polycrystalline silicon film 6b on the element isolation/insulation film4 into discrete portions.

Subsequently, after removing the silicon oxide films 31, 32 by HF, a silicon oxide film 33 is stacked on the entire surface by low-pressure CVD as shown in Figs. 11A and 11B.

This silicon oxide film 33, after deposition, is heated in an O_2 atmosphere at 1000°C and thereby changed to a compact oxide film without movements of electric charges, or the like. The silicon oxide film 33, as well as the second gate insulating film 7, functions as a gate insulating film, and functions as an insulating film that protects side surfaces of the polycrystalline silicon film 6b.

After that, as shown in Figs. 12A and 12B, the polycrystalline silicon film 8a and the WSi film 8b are sequentially stacked, then patterned in the same manner as the foregoing embodiment to form control gates 8 and floating gates 6 and the source drain diffusion layers 12 are made.

Also in this embodiment, similarly to the foregoing embodiment, the gate insulating film is cut and separated at device-isolating regions. Therefore, excellent data holding property is obtained.

[Embodiment 3]

Figs. 13A, 13B through Figs. 16A, 16B show a manufacturing process according to a still another embodiment. Although the former embodiment, as shown in Figs. 5A and 5B, sequentially stacked the second-layer polycrystalline silicon film 6b and the second gate insulating film 7, the embodiment shown here stacks makes slits 13 for separating the second-layer polycrystalline silicon film 6b above the element isolation/insulation films 4 before stacking the second gate insulating film 7 as shown in Figs. 13A and 13B. The second gate insulating film 7 is stacked thereafter. Then, a resist pattern (not shown) having the same apertures as the slits 13 is applied on the second gate insulating

film 6b, and the second gate insulating film 6b is etched by RIE and separated at portions of the slits 13 as shown in Figs. 14A and 14B. After that, in the same manner as the former embodiment, the phosphorus-doped polycrystalline silicon film 8a is stacked as a gate electrode material film by CVD, and the WSi film 8b is successively stacked thereon.

Subsequently, by providing a pattern of a resist, the WSi film 8b, polycrystalline silicon film 8a, gate insulating film 7, polycrystalline silicon films 6b, 6a and gate insulating film 5 are sequentially etched by RIE so as to pattern the control gate 8 into continuous word lines WL and simultaneously separate the floating gate 6 into discrete memory cells in the bit-line direction. Then, by introducing ions, source and drain diffusion layers 12 for respective memory cells are made in self-alignment with the control gates8.

This embodiment also separates the second gate insulating film 7 on the floating gates 6 above the element isolation/insulation films 4, and provides excellent data-holding property equivalent to the former embodiments.

[Embodiment 4]

All embodiments explained heretofore cut and separate the second gate insulating film 7 above the element isolation/insulation films 4. The instant embodiment, however, is intended to obtain substantially the same effect without cutting and separating it. Cross-sectional aspects of this embodiment are shown in Figs. 17A and 17B, which correspond to Figs. 2A and 2B.

The structure shown in Figs. 17A and 17B is different from that of Figs. 2A and 2B in making slits 13 for separating the floating gate 6 above the element isolation/insulation films 4 prior to stacking the second gate insulating film 7 and simultaneously conducting recess-etching of the element isolation/insulation films 4 to make recesses 41. Therefore, the first gate insulating film 7 is disposed along the recesses formed on surfaces of the element isolation/insulation films 4.

As shown in Fig. 17A, assigning a to the width of each slit 13 and hence the width of each recess 41 formed into each element

isolation/insulation film 4, and b to the depth of each recess 41, distance between adjacent floating gates is substantially a+2b. By adjusting this distance to a value diminishing movements of electric charges between floating gates to a negligible value, excellent data-holding property equivalent to that of the foregoing embodiments can be obtained.

A specific manufacturing process according to this embodiment is explained with reference to Figs. 18 through 25, taking the cross-section of Fig. 17A into account. As shown in Fig. 18, a silicon oxide film, approximately 8 nm thick, is formed as the first gate insulating film 5 on a silicon substrate 1, and the first polycrystalline silicon film 6a is stacked thereon up to a thickness around 60 nm by low-pressure CVD. Successively, a 150 nm thick silicon nitride film 21a and a 165 nm thick silicon oxide film 21b are stacked by low-pressure CVD.

Subsequently, after conducting oxidation by combustion of hydrogen at 850°C for 30 minutes, a resist pattern is formed to cover the device-isolating regions by lithography, and the silicon oxide film 21b and the silicon nitride film 21a are etched by RIE to make a patterned mask. Using this mask, the polycrystalline silicon film 6a and the gate insulating film 5 are etched by RIE, and the silicon substrate 1 is additionally etched, thereby to make the device isolating grooves 3. As a result, stripe-shaped element-forming regions 2 are defined.

Subsequently, after making a thermal oxide film on sidewalls of the device isolating grooves 3, a silicon oxide film 4 is stacked by plasma CVD, and then flattened by CMP, thereby to bury the device isolating grooves 3 with it as shown in Fig. 19. The silicon oxide film 21b is removed by buffering fluoric acid, and the silicon nitride film 21a is removed by treatment using phosphoric acid at 150°C for 30 minutes, thereby to obtain the state of Fig. 20.

After that, as shown in Fig. 21, the second polycrystalline silicon film 6b, 100 nm thick, is stacked by low-pressure CVD. After that, as shown in Fig. 22, a silicon oxide film 42 is stacked to a thickness around 230 nm by low-pressure CVD, and through lithography and RIE, apertures 13' for making slits are made.

Further, as shown in Fig. 23, a silicon oxide film 43, approximately 70 nm thick, is stacked by low-pressure CVD, and by an etch-back process, it is maintained as side spacers only on side walls of the apertures 13'.

After that, using the silicon oxide films 42, 43 as a mask, the polycrystalline silicon film 6b is etched by RIE to make slits 13 for isolating floating gates, as shown in Fig. 24. Furthermore, surface of the element isolation/insulation film 4 is etched by RIE having a large selectivity relative to the polycrystalline silicon, thereby to make recesses 41 of the same width as that of slits 13 in the element isolation/insulation film 4.

Subsequently, after removing the silicon oxide films 42, 43 by treatment using O_2 plasma and HF, the second gate insulating film 7 in form of 17 nm thick ONO film is stacked as shown in fig. 25, and successively thereafter, a 100 nm thick third polycrystalline silicon film 8a by low-pressure CVD and a 50 nm thick WSi film 8b by plasma CVD are sequentially stacked.

Thereafter, although not shown, through the same steps as those of the foregoing embodiments, gate portions are divided into discrete memory cells, and source and drain diffusion layers are formed.

Fig. 26 shows correlations between slit width separating adjacent floating gates and number of defective bits occurring upon movements of electric charges between floating gates. Arrows in Fig. 26 show the range of variance in number of defective bits, and the curve connecting their average values. It is observed that miniaturization of memory cells to enhance the density to the extent decreasing the slit width to 0.14 μm or less invites a serious increase of defective bits. According to the embodiment shown here, substantial slit width can be a+2b by the depth b of the recess in the element isolation/insulation film 4 relative to the slit width a on the plane. More specifically, in a 256 Mbit NAND type EEPROM, if specifications about defective bits require 2 bits/chip, at least 0.14 μm is required as the slit width. In this embodiment, therefore, by making the recess 41 to satisfy $a+2b>0.14$ [μm], that specification can be satisfied.

In EEPROM according to the invention described above, by separating second gate insulting films between floating gates and control gates above element isolation/insulation films between adjacent memory cells interposing the element isolation/insulation film between them, movements of electric charges between adjacent floating gates can be prevented. Alternatively, even without fully separating the second gate insulating film above device isolating films, by making recesses into surfaces of the element isolation/insulation films and allowing the second gate insulating film to be continuous along the recesses, distance between adjacent floating gates increases substantially, and movements of electric charges between adjacent floating gates can be prevented. Therefore, even when memory cells are microminiaturized, data destruction caused b movements of electric charges can be prevented.